ABSTRACT OF THE DISCLOSURE

A clock ratio data synchronizer is provided that utilizes a plurality of flip flops to synchronize data received by the synchronizer from first clock domain logic at a first clock frequency to a clock frequency of second clock domain logic. Each flip flop is capable of sampling data only on an edge of a clock and outputting data only on an edge of the clock. By utilizing flip flops in the synchronizer, data values are only allowed to change on clock edges. This, in turn, greatly improves clock skew tolerance, and also setup time margins for the first clock domain logic and for the second clock domain logic.